What is claimed is:

1. An input buffer, comprising:

a pull-up transistor connected between a power supply voltage and an input pad and having a gate to which a control voltage is applied, and having a substrate to which a floating well voltage is applied;

a transmission transistor having a gate to which the power supply voltage is applied and a substrate connected to a ground voltage, and transmitting a signal applied to the input pad;

a buffer generating an input signal by buffering the signal transmitted by the transmission transistor; and

a controller generating the voltage of the signal applied to the input pad as the control voltage and the floating well voltage when a high voltage is applied to the input pad, generating the ground voltage as the control voltage in the case where a voltage less than the high voltage is applied to the input pad, and generating the power supply voltage as the floating well voltage.

2. The input buffer of claim 1, wherein the high voltage is greater than the power supply voltage.

3. The input buffer of claim 1, wherein the controller comprises:

a high voltage detecting circuit generating a high voltage detecting signal when the high voltage is applied to the input pad;

a high voltage detecting reset circuit generating a high voltage detecting reset signal for resetting the high voltage detecting signal, when the voltage less than the high voltage is applied to the input pad; and

a control voltage and floating well voltage generating circuit generating the voltage applied to the input pad as the control voltage and the floating well voltage when the high voltage detecting signal is generated, and generating the ground voltage as the control voltage and the power supply voltage as the floating well voltage when the high voltage detecting signal is reset.

4. The input buffer of claim 3, wherein the high voltage detecting circuit comprises:

a first PMOS transistor connected between the input pad and a first node and having a gate to which the power supply voltage is applied, and having a substrate to which the floating well voltage is applied;

a first NMOS transistor connected between the first node and a second node and having a gate to which the power supply voltage is applied, and having a substrate to which the ground voltage is applied;

a second NMOS transistor having a drain connected to the second node, a gate to which the high voltage detecting reset signal is applied, and a source and a substrate connected to the ground voltage;

a second PMOS transistor having a source and a substrate connected to the power supply voltage, and a gate connected to the first node;

a third PMOS transistor having a source connected to a drain of the second PMOS transistor, a gate connected to the second node, and a substrate connected to the power supply voltage; and

a third NMOS transistor having a gate connected to the second node, a drain connected to a drain of the third PMOS transistor, and a source and a substrate connected to the ground voltage; and

wherein the high voltage detecting signal is generated at the drain of the third PMOS transistor.

5. The input buffer of claim 3, wherein the high voltage detecting reset circuit comprises:

a fourth NMOS transistor connected between the input pad and a third node and having a gate to which the power supply voltage is applied, and having a substrate connected to the ground voltage;

a fourth PMOS transistor having a source and a substrate to which the power

supply voltage is applied, and a gate connected to the input pad;

a fifth PMOS transistor having a source connected to a drain of the fourth PMOS transistor, a substrate to which the power supply voltage is applied, and a gate connected to the third node; and

a fifth NMOS transistor having a drain connected to a drain of the fifth PMOS transistor, a gate connected to the third node, and a source and a substrate connected to the ground voltage; and

wherein the high voltage detecting reset signal is generated at the drain of the fifth PMOS transistor.

6. The input buffer of claim 3, wherein the control voltage and floating well voltage generating circuit comprises:

a sixth PMOS transistor having one of a source and drain to which the power supply voltage is applied, a gate connected to a fourth node, and the other of the drain and source and a substrate to which the floating well voltage is applied;

a seventh PMOS transistor having one of a source and drain connected to the fourth node, a gate to which the power supply voltage is applied, the other of the drain and source connected to the input pad, and a substrate to which the floating well voltage is applied;

an eighth PMOS transistor having a gate connected between the fourth node

and the input pad and to which the power supply voltage is applied, and having a substrate to which the floating well voltage is applied;

a sixth NMOS transistor having a gate to which the power supply voltage is applied, a drain connected to the fourth node, and a substrate connected to the ground voltage; and

a seventh NMOS transistor having a drain connected to a source of the sixth NMOS transistor, a gate to which the high voltage detecting signal is applied, a substrate and a source connected to the ground voltage; and

wherein the control voltage is generated at the fourth node and the floating well voltage is generated at the one of the drain and source of the sixth PMOS transistor.

7. An input buffer, comprising:

a pull-up transistor connected between a power supply voltage and an input pad;

a transmission transistor having a gate to which the power supply voltage is applied and a substrate connected to a ground voltage, and transmitting a signal applied to the input pad;

a buffer generating an input signal by buffering the signal transmitted by the transmission transistor; and

a controller turning off the pull-up transistor when a high voltage is applied to the input pad, and turning on the pull-up transistor in the case where a voltage less than the

high voltage is applied to the input pad.

8. The input buffer of claim 7, wherein the controller comprises:

a high voltage detecting circuit generating a high voltage detecting signal when the high voltage is applied to the input pad, and resetting the high voltage detecting signal in the case where a voltage less than the high voltage is applied to the input pad; and

a control voltage and floating well voltage generating circuit applying a voltage applied to the input pad to a gate and a substrate of the pull-up transistor when the high voltage detecting signal is generated, and applying the ground voltage and the power supply voltage to the gate and the substrate of the pull-up transistor in the case where the high voltage detecting signal is reset.

9. The input buffer of claim 8, wherein the high voltage detecting circuit comprises:

a high voltage detecting circuit generating a high voltage detecting signal when a high voltage is applied to the input pad; and

a high voltage detecting reset circuit generating a high voltage detecting reset signal for resetting the high voltage detecting signal, in the case where a voltage less than the high voltage is applied to the input pad.

10. The input buffer of claim 9, wherein the high voltage detecting circuit comprises:

a first PMOS transistor connected between the input pad and a first node and having a gate to which the power supply voltage is applied, and having a substrate to which the floating well voltage is applied;

a first NMOS transistor connected between the first node and a second node and having a gate to which the power supply voltage is applied, and having a substrate to which a ground voltage is applied;

a second NMOS transistor having a drain connected to the second node, a gate to which the high voltage detecting reset signal is applied, and a source and a substrate connected to the ground voltage;

a second PMOS transistor having a source and a substrate connected to the power supply voltage, and a gate connected to the first node;

a third PMOS transistor having a source connected to a drain of the second PMOS transistor, a gate connected to the second node, and a substrate connected to the power supply voltage; and

a third NMOS transistor having a gate connected to the second node, a drain connected to a drain of the third PMOS transistor, and a source and a substrate connected to the ground voltage; and

wherein the high voltage detecting signal is generated at the drain of the third PMOS transistor.

11. The input buffer of claim 9, wherein the high voltage detecting reset circuit comprises:

a fourth NMOS transistor connected between the input pad and third node and having a gate to which the power supply voltage is applied, and having a substrate connected to the ground voltage;

a fourth PMOS transistor having a source and a substrate to which the power supply voltage is applied, and a gate connected to the input pad;

a fifth PMOS transistor having a source connected to a drain of the fourth PMOS transistor, a substrate to which the power supply voltage is applied, and a gate connected to the third node; and

a fifth NMOS transistor having a drain connected to a drain of the fifth PMOS transistor, a gate connected to the third node, and a source and a substrate connected to the ground voltage; and

wherein the high voltage detecting reset signal is generated at the drain of the fifth PMOS transistor.

12. The input buffer of claim 8, wherein the control voltage and floating well

voltage generating circuit comprises:

a sixth PMOS transistor having one of a source and drain to which the power supply voltage is applied, a gate connected to a fourth node, the other of the drain and source to which the floating well voltage is applied, and a substrate;

a seventh PMOS transistor having one of a source and drain connected to the fourth node, a gate to which the power supply voltage is applied, the other of the drain and source connected to the input pad, and a substrate to which the floating well voltage is applied;

an eighth PMOS transistor having a gate connected between the fourth node and the input pad and to which the power supply voltage is applied, and a substrate to which the floating well voltage is applied;

a sixth NMOS transistor having a gate to which the power supply voltage is applied, a drain connected to the fourth node, and a substrate connected to the ground voltage; and

a seventh NMOS transistor having a drain connected to a source of the sixth NMOS transistor, a gate to which the high voltage detecting signal is applied, and a substrate and a source connected to the ground voltage; and

wherein the control voltage is generated through the fourth node and the floating well voltage is generated through the drain or source of the sixth PMOS transistor.